

Searches for User *nguyenl* (Count = 8790)

Queries 8741 through 8790.

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S #	Updt	Database	Query	Time	Comment
<u>S8790</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	(set adj index) adj2 (bit)	2006-01-25 13:00:59	
<u>S8789</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	(set) adj index	2006-01-25 12:42:03	
<u>S8788</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	(711/\$.ccls.) and (set adj2 bit and tag adj2 bit)	2006-01-25 12:33:01	
<u>S8787</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	(set adj2 bit) and (tag adj2 bit)	2006-01-25 12:32:46	
<u>S8786</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	(tag) adj2 (bit)	2006-01-25 12:31:42	
<u>S8785</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	(set) adj2 (bit)	2006-01-25 12:30:48	
<u>S8784</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	bit	2006-01-25 12:30:21	
<u>S8783</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	tag	2006-01-25 12:28:03	
<u>S8782</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	set	2006-01-25 12:27:46	
<u>S8781</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	711/\$.ccls.	2006-01-25 12:27:21	
<u>S8780</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	((pick\$ or select\$ or choos\$) near3 (eras\$ near2 block or eras\$ near2 page)) and (time near2 eras\$ near2 block) and (time near2 eras\$ near2 page)	2006-01-24 14:43:32	
<u>S8779</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	(pick\$ or select\$ or choos\$) near3 ((eras\$ near2 block) or (eras\$ near2 page))	2006-01-24 14:41:10	
<u>S8778</u>	<u>U</u>	PGPB,USPT,EPAB,JPAB,DWPI,TDBD	(time near2 eras\$ near2 page) and (time near2 eras\$ near2 block)	2006-01-24	


Results for "((config* index)<in>metadata)"

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» Key

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information

- ☐
- 1. Reducing cache misses by application-specific re-configurable indexing**
Patel, K.; Macii, E.; Benini, L.; Poncino, M.;
Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conference on
7-11 Nov. 2004 Page(s):125 - 130
[AbstractPlus](#) | Full Text: [PDF\(783 KB\)](#) IEEE CNF
 - 2. Inverse kinematics of planar redundant manipulators using virtual link and displacement distribution schemes**
Chung, W.J.; Chung, W.K.; Youm, Y.;
Robotics and Automation, 1991. Proceedings., 1991 IEEE International Conference on
9-11 April 1991 Page(s):926 - 932 vol.1
Digital Object Identifier 10.1109/ROBOT.1991.131707
[AbstractPlus](#) | Full Text: [PDF\(456 KB\)](#) IEEE CNF


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IEEE JNL	IEEE Journal or Magazine
IEEE JNL	IEEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEEE CNF	IEEE Conference Proceeding
IEEE STD	IEEE Standard


1. Array tags in forestry

Little, W.; Baker, P.; Fraser, D.; Aune, J.; Sauder, B.;
Communications, Computers and Signal Processing, 1991., IEEE Pacific Rim Conference on
9-10 May 1991 Page(s):721 - 724 vol.2
Digital Object Identifier 10.1109/PACRIM.1991.160841

[AbstractPlus](#) | Full Text: [PDE\(284 KB\)](#) IEEE CNF


Results for "((config* cache)<in>metadata)"

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IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information

- ☐ **1. Fast configurable-cache tuning with a unified second-level cache**
 Gordon-Ross, A.; Vahid, F.; Dutt, N.;
 Low Power Electronics and Design, 2005. ISLPED '05. Proceedings of the 2005 International Symposium on
 8-10 Aug. 2005 Page(s):323 - 326
[AbstractPlus](#) | Full Text: [PDF\(305 KB\)](#) IEEE CNF
- ☐ **2. Energy-efficiency potential of a phase-based cache resizing scheme for embedded systems**
 Pokam, G.; Bodin, F.;
 Interaction between Compilers and Computer Architectures, 2004. INTERACT-8 2004. Eighth Workshop on
 15 Feb. 2004 Page(s):53 - 62
 Digital Object Identifier 10.1109/INTERA.2004.1299510
[AbstractPlus](#) | Full Text: [PDF\(2178 KB\)](#) IEEE CNF
- ☐ **3. Automatic tuning of two-level caches to embedded applications**
 Gordon-Ross, A.; Vahid, F.; Dutt, N.;
 Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings Volume 1, 16-20 Feb. 2004 Page(s):208 - 213 Vol.1
 Digital Object Identifier 10.1109/DATE.2004.1268850
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- ☐ **4. A self-tuning cache architecture for embedded systems**
 Chuanjun Zhang; Vahid, F.; Lysecky, R.;
 Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings Volume 1, 16-20 Feb. 2004 Page(s):142 - 147 Vol.1
 Digital Object Identifier 10.1109/DATE.2004.1268840
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- ☐ **5. A highly configurable cache architecture for embedded systems**
 Zhang, C.; Vahid, F.; Najjar, W.;
 Computer Architecture, 2003. Proceedings. 30th Annual International Symposium on 9-11 June 2003 Page(s):136 - 146
 Digital Object Identifier 10.1109/ISCA.2003.1206995
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- ☐ **6. Configuration caching management techniques for reconfigurable computing**
 Li, Z.; Compton, K.; Hauck, S.;
 Field-Programmable Custom Computing Machines, 2000 IEEE Symposium on 17-19 April 2000 Page(s):22 - 36
 Digital Object Identifier 10.1109/FPGA.2000.903390
[AbstractPlus](#) | Full Text: [PDF\(1132 KB\)](#) IEEE CNF

7. **Highly scalable parallel parametrizable architecture of the motion estimator**
Cmar, R.; Vernalde, S.;
European Design and Test Conference, 1997. ED&TC 97. Proceedings
17-20 March 1997 Page(s):208 - 212
Digital Object Identifier 10.1109/EDTC.1997.582360
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8. **CMOS PA-RISC processor for a new family of workstations**
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25 Feb.-1 March 1991 Page(s):202 - 207
Digital Object Identifier 10.1109/CMPCON.1991.128807
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9. **Association rule based data mining agents for personalized Web caching**
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10. **An efficient external-memory implementation of region query with application to area routing**
Liao, S.; Shenoy, N.; Nicholls, W.;
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16-18 Sept. 2002 Page(s):36 - 41
Digital Object Identifier 10.1109/ICCD.2002.1106744
[AbstractPlus](#) | Full Text: [PDF](#)(260 KB) IEEE CNF
11. **Managing multi-configuration hardware via dynamic working set analysis**
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12. **Cache design and exploration for low power embedded systems**
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Performance, Computing, and Communications, 2001. IEEE International Conference on.
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13. **Memory design and exploration for low power, embedded systems**
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14. **Hybrid data/configuration caching for striped FPGAs**
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15. **Reconfigurable processor architectures exploiting high bandwidth optical channels**
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